FLIP-CHIP PACKAGING

This application is a Continuation of 10/215,570, filed 08/09/2002, Patent number 6,747,342

BACKGROUND OF THE INVENTION

Related Applications

The following copending U.S. patent application Serial No. 09/430,500, "NOVEL JFET STRUCTURE AND MANUFACTURE METHOD FOR LOW ON RESISTANCE AND LOW VOLTAGE APPLICATIONS", Ho-Yuan Yu, filed 2 December 1999, is incorporated herein by reference for all purposes. The following copending U.S. patent application Serial No. 09/708,336, "STARTER DEVICE FOR NORMALLY "OFF" JFETS", Ho-Yuan Yu, filed 7 November 2000, is incorporated herein by reference for all purposes. The following copending U.S. patent application Serial No. 09/708,336, "SEMICONDUCTOR PACKAGE FOR POWER JFET HAVING COPPER PLATE FOR SOURCE AND WIRE BOND OR RIBBON CONTACT FOR GATE", Ho-Yuan Yu, filed 2 March, 2001, is incorporated herein by reference for all purposes.

FIELD OF THE INVENTION

The present invention is related to semiconductor packaging including the manner in which a semiconductor die is mechanically connected to a supporting structure as well as the methods used for making electrical connections to electrode pads on the die.